REMARKS

Claims 1-20 are pending in the present application. Claim 1 has been amended to correct and inadvertent error. Reconsideration of the rejection of the application is respectfully requested in view of the following remarks.

The Claims Are Allowable Over the Prior Art

Claims 1-14 and 17-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,860,017 to Sharangpani ("Sharangpani").

Embodiments of the present invention refer to branch misprediction recovery. In one embodiment, an instruction that is predicted not to be executed is advanced through an instruction pipeline. It can be stored in a mispredicted path side memory and then restored as a result of a branch misprediction. Having the instruction in the path side memory allows it to be executed faster compared to prior art methods of handling branch misprediction where the correct instructions need to be retrieved from system memory.

Sharangpani refers to speculative execution of instructions. As indicated at Col. 3, line 41 to Col. 4, line 30, the processor looks for front-end and back resources that are available and inserts instructions from a second target into the execution pipeline. As indicated at Col. 4, lines 23-30, "[o]nce the condition of the conditional branch instruction is resolved, instructions from the incorrect stream are canceled while instructions from the correct instruction stream continue through any additional processing stages. Valid, executed instruction are subsequently retired

and committed to architectural state. In this manner, the performance penalty incurred for branch mispredictions is significantly reduced if not eliminated." Sharangpani is clear that instructions from the second target are inserted into and continue through processing stages along with instructions from the first target. No mispredicted path side memory is described by Sharangpani.

The Office Action concedes that such a memory is not expressly detailed in Sharangpani, but states that Sharangpani teaches, "executing the predicted to be executed path of instructions and the predicted not to be executed path of instructions in parallel and when the branch was resolved using the path of the two paths that was correct according to the resolution of the branch and flushing the incorrect path." The Office Action also talks of how Sharangpani describes memory such as cache and main memory and that "one of ordinary skill would have been motivated to separately store the results from the each pipeline path so that the deleting of results from the incorrect path would be performed easily for efficiently executing the branch." The support for this teaching is Col. 7, lines 32-59, Col. 3, line 41 to Col. 4, line 30 (addressed above); and Col. 11, lines 25-59.

Col. 7, lines 32-59 refer to a specific feature of Sharangpani, which is to select a second target based on branches that are "unlikely to be predicted accurately." Since 1 in 5 instructions may be a branch instruction, using resources to process all second target instructions would be wasteful and impact performance. Col. 11, lines 25-39, refer to a table that indicates what instruction streams are "live." When a branch instruction is executed, those instructions from the non-taken branch are no longer needed and processing of those instructions is discarded. The table is also updated to indicate that this stream of instruction is no longer live, preventing more instructions from this stream being fetched from memory.

The cited sections to do not teach or suggest a mispredicted path side memory in parallel to the execution instruction pipeline as called for in the claims. Though it is true that "memory" is well known in the art, the prior art does not teach the use of memory in a manner expressed by the claims. For example, cache and main memory is for supplying instructions to the instruction pipeline, but is not used for storing results of execution in the pipeline. In Sharangpani, the instruction pipeline is shown in Fig. 3 with elements such as 306, 307, 308, 310 and 320. The instructions travel in this pipeline unless they are halted due to execution of a branch being taken. Sharangpani is clear that instructions in the mispredicted branch continue with execution in the pipeline. The presently claimed invention, however, refers to restoring results stored in the mispredicted path side memory. Thus, the presently claimed invention refers to a storage of results that is separate from any momentary storage that occurs within the pipeline units. As indicated above, nothing in Sharangpani teaches such a memory. Accordingly, reconsideration and withdrawal of the rejection of claims 1-14 and 17-20 under 35 U.S.C. § 103(a) is respectfully requested.

Conclusion

Applicant respectfully requests entry of the above amendments and favorable action in connection with this application.

The Examiner is invited to contact the undersigned to discuss any matter concerning this application.

The Office is hereby authorized to charge any fees required under 37 C.F.R. §§ 1.16 or 1.17 or credit any overpayment to Kenyon and Kenyon Deposit Account No. 11-0600.

Respectfully submitted,

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